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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,741	08/28/2003	Yoshiyuki Arai	60188-598	5729

7590 03/07/2005
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Washington, DC 20005-3096

EXAMINER

ROMAN, ANGEL

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/649,741	Applicant(s) ARAI ET AL.	
	Examiner Angel Roman	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) 7-12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☒ Claim(s) 3-6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>08/28/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I claims 1-6 in the reply filed on 02/16/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. It is suggested that Applicants cancel non-elected claims 7-12 in response to this office action.

Information Disclosure Statement

3. The examiner has considered the reference cited in the information disclosure statement filed 08/28/03.

Oath/Declaration

4. The Oath documents filed 08/28/03 are acceptable.

Drawings

5. The drawings filed 08/28/03 are acceptable.

Specification

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

8. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Dotta et al. U.S. Patent 6,353,263 B1.

Regarding claim 1, Dotta et al. discloses a semiconductor device comprising; a substrate 3 having an electrode pad 4; a first semiconductor chip 1 mounted on the substrate 3 with a first adhesion layer 20 interposed therebetween; a second semiconductor chip 2 mounted on the first semiconductor chip 1 with a second adhesion layer 7 interposed therebetween and having an electrode pad 18 on an upper surface thereof; a wire 8 for bonding the electrode pad 4 of the substrate 3 and the electrode pad 18 of the second semiconductor chip 2 to each other; and a mold resin 9 sealing therein the first and second semiconductor chips (1, 2) and the wire 8, the first adhesion layer 20 having a peripheral edge portion 21 protruding outwardly from the first semiconductor chip 1, the second semiconductor chip 2 having a peripheral edge portion protruding outwardly beyond a peripheral edge portion of the first semiconductor chip 1 (see figure 4(b)).

Regarding claim 2, Dotta et al. discloses the peripheral edge portion of the second semiconductor chip 2 is protruding outwardly beyond the peripheral edge portion of the first adhesion layer 20 (see figure 1).

Allowable Subject Matter

9. Claims 3-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record either singularly or in combination failed to anticipate or render obvious the limitations of disclosing a center of the second semiconductor chip being offset from a center of the first semiconductor chip as required by claim 3.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mori and Haba et al. disclose semiconductor devices having a second semiconductor chip stacked on a first semiconductor chip, wherein the second semiconductor chip is offset from a center of the first semiconductor chip. Tamaki et al. and Arai et al. disclose semiconductor devices having stacked semiconductor chips wherein the first chip has an adhesion layer having a protruding peripheral edge portion with larger protrusion and surface height than a first edge portion (see figure 20A). Fukui et al. discloses a semiconductor device having stacked semiconductor chips with a top chip having a protruding peripheral edge portion outwardly from a first semiconductor chip (see figure 10). Shimoda discloses a semiconductor device having plural stacked semiconductor chips (see figure 3).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
March 1, 2005


MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER